REMARKS

The application was filed on 28 June 2001 with fifteen claims. The Examiner on 21 April 2004 issued a first Action. In the action, the Examiner objected to the drawings stating the branch information queue jof claims 5 and 6 must be shown in the figures or cancelled from the claims. The Examiner issued several objections to the specification and the title. With respect to the claims, the Examiner objected to claim 5 and rejected claims 1-10 under 35 U.S.C. §112. The Examiner issued four art rejections of the claims: he rejected claims 1, 5, 10-12 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 6,629,271B1 entitled TECHNIQUE FOR SYNCHRONIZING FAULTS IN A PROCESSOR HAVING A REPLAY SYSTEM to Lee et al. (Lee '271); he also rejected claims 2-4, 6 under 35 U.S.C. §103(a) as being unpatentable over Lee '271 in view of U.S. Patent No. 6,311,261 entitled APPARATUS AND METHOD FOR IMPROVING SUPERSCALAR PROCESSORS to Chamdani et al. (Chamdani '261) and U.S. Patent Application Publication 2002/0078317 A1 entitled FIRST-IN, FIRST-OUT (FIFO) MEMORY WITH MOVING BOUNDARY to Yasoshima (Yasoshima '317 Pub); he further rejected claims 7-9 under 35 U.S.C. §103(a) as being unpatentable over Yasoshima '317 Pub in view of Lee '271; and issued a last rejection of claims 13-15 under 35 U.S.C. §103(a) as being unpatentable over Lee '271.

Applicants respond. Applicants amended the title and the specification and submit a proposed amendment to the drawing. Also, independent claims 1, 6, 7, 10, 11, and 13 and dependent claims 5, 9, and 15 are amended; claims 2 and 14 are cancelled. Claims 1, 2-13, and 15 are pending.

The Objection to the specification, title, claim 5 and the Rejection of claims 1-10 under 35 U.S.C. §112, second paragraph

Applicants have amended the specification, making the corrections to the various headings, correction of serial number of a reference patent, providing figure numbers for a reference to the FIGS. and changing the title of the application as suggested by the Examiner.

Applicants submit a Proposed Amendment to the Drawing amending Figure 2 to insert a branch information queue and its reference numeral 252. In submitting the proposed amendment, Applicant has not added new matter. Support for the branch information queue 252 is given in the originally filed specification on page 22, line 3 and again on page 22, line 12, and in claims 5, 6. With respect to the objection regarding step 830 on figure 8, Applicants amend figure 8 to show that if the bank number is not at the maximum bank number at step 830, then the process moves to step 836 where the process determines if the free entry is valid. In doing so, Applicants have not added new matter - because the free pointer is at a tail pointer; is not at a head pointer; so logically the next determination is whether the free entry, i.e., the tail pointer, already contains valid data, as in step 836.

The Rejection Under 35 U.S.C. §102(b) over Lee '271

The Examiner rejected claims 1, 5, 10-12 as being anticipated by Lee '271. In response, Applicants have amended independent claims 1, 5, 10 and 11. The amendments have narrowed the claims to particularly point out and distinctly claim that the invention has a resource that is shared between hardware threads in a multithreaded processor, wherein entries for different threads are interspersed among each other and the first entry of a particular thread is allowed to wrap around its last entry.

In doing so, Applicants incorporated the limitations of claim 2 into claim 1. In issuing a rejection of claim 2 under 35 U.S.C. §103(a), the Examiner admitted that Lee '271 cannot anticipate the amended claims. Certainly, the Examiner is correct by not rejecting the original claim 2 as being anticipated by Lee '271 because Lee '271 does not

show that a first entry pertaining to a first thread can wrap around its last entry in a shared resource having interspersed entries among the various threads. Applicants respectfully request the Examiner to withdraw the rejection of claims 1, 5, 10-12 under 35 U.S.C. §102(e) as being anticipated by Lee '271.

The Rejection of claims 2-4, 6 Under 35 U.S.C. §103(a) over Lee '271, Chamdani j'261 and Yasoshima '317 Pub

The Examiner rejected claims 2-4 and 6 under 35 U.S.C. §103(a) under a combination of Lee '271, Chamdani '261 and Yasoshima '317 Pub.

The Examiner asserts that Lee '271 teaches a multithreaded processor having shared resources wherein entries for one thread are interspersed among entries of another thread. Chamdani '261 teaches a circular buffer having head and tail pointers while Yasohima '317 Pub teaches that resources of one data segment B can wrap around resources of another data segment A. Reserving the argument that Lee '271 does not teach interspersed entries among the threads, Applicants concur with the above statement of Chamdani '261 and Yasoshima '317 Pub.

Applicants, however, traverse on the Examiner's assertion that it would be obvious to modify Lee '271 with a circular buffer of Chamdani '261 and the wrap-around feature of Yasoshima '317 Pub and still derive Applicants' invention. First, the Examiner admits that none of the references teach the claimed limitation that the first entry of one thread is capable of wrapping around the last entry of the same thread. The Examiner provides this limitation with hindsight and with Applicants' teachings.

In addressing the rejection, Applicants assert two points. First, Yashoshima '317 Pub was not intended to be used with simultaneous multithreading and thence teaches against its combination with Lee '271 and Chamdani '261. Second, Applicants show that Yasoshima '317 Pub does not teach that the first entry of one thread is capable of wrapping around the last entry of the same thread. With respect to the first point, Applicants refer to Yashoshima '317 Pub at column 3, lines 1-8 which states, "Specifically, assuming the tasks generating data A and data B are not continuously performed simultaneously, when performing task A, data A will likely require a

majority of space in the FIFO memory, and visa versa, when task B is performed. The present invention allows for the allocation of the memory to be predominately for use by FIFO A at a given time, and by FIFO B at a separate time." (Emphasis added) In other words, Yashoshima '317 Pub specifically teaches away from using its FIFO for simultaneous multithreading. Respectfully, the Examiner may not assert a use into a reference which specifically teaches against that use.

With respect to the second point: Yashoshima '317 Pub does not teach that the write pointer of FIFO B can wrap around itself or, in the language of Yashoshima '317 Pub, the read point of FIFO B; Yashoshima '317 Pub teaches only that FIFO B can wrap around FIFO A, *see* Figures Fig. 4(e) through 4(h). Yashoshima '317 Pub solves only one-half of the problem, i.e., that of allocation of unused memory for two data segments; it does not address and is completely silent on the other half of the problem: more specifically, how to keep track of how many times FIFO B wraps around itself in order to maintain in-order processing in an out-of-order multithreaded processor. Because Yashoshima '317 Pub teaches against simultaneous multithreading and is silent about maintaining instruction order in an out-of-order processor, Applicants assert that the Examiner fails to create a prima facie case of obviousness under 35 U.S.C. §103(a). The references themselves must suggest their combination!

The Rejection of claims 7-9 under 35 U.S.C. § 103(a) over Yasoshima '317 Pub and Lee '271

The Examiner also rejected claims 7-9 as being obvious in view of Yashoshima '317 Pub and Lee '271. Applicants respectfully traverse this rejection in view of the amendments and in view of the claim limitation of claim 7 of "incrementing a bank number if the first entry passes a last entry of the particular thread before it finds the free entry." As discussed above, Yashoshima '317 Pub does not teach how FIFO B can wrap itself, only how FIFO B can wrap FIFO A. In fact, it stands to reason that Yashoshima '317 teaches the boundaries of FIFO B and FIFO A to be dynamic to avoid FIFO B wrapping around itself; in other words, why change the boundaries of FIFO A if FIFO B can wrap itself and find the next available memory space?

Applicants respectfully assert that Yashoshima '317 does not teach that given FIFO B, the first entry of FIFO B cannot wrap/pass the last entry FIFO B before finding available memory space. Applicants further request that the Examiner withdraw the rejection of claims 7-9 under the 35 U.S.C. §103(a) in view of Yashoshima '317 Pub and Lee '271.

The Rejection of claims 13-15 under 35 U.S.C. §103(a) over Lee '271

The Examiner rejected claims 13-15 as being obvious over Lee '271. Applicants have amended independent claim 13 to incorporate the limitation of cancelled claim 14 and have inserted the further limitation that the number of times that the head pointer in one of the entries wraps around/passes the tail pointer of the same thread in another of the entries is recorded. Lee '271 does not teach this limitation, and the Examiner has admitted as much when he said Lee '271 does "not teach a first entry of one thread being capable of wrapping around the last entry of the same thread .... at least one free pointer for the at least one thread indicating an entry in the queue available for resources of the at least one thread." Lee '271, moreover, does not suggest such a modification. For that modification, the Examiner relied on Yashoshima '317 Pub, which modification is not proffered by the Examiner is the current rejection of claims 13-15 and which supposed combination is addressed above. Thus, Applicants request the Examiner to withdraw the rejection of claims 13-15 under 35 U.S.C. §103(a) over Lee '271. In view of the amendments and the remarks, Applicants request the Examiner to allow the claims.

Conclusion

Applicants maintain that the combination of Lee '271 and/or Chamdani '261 and/or Yashoshima '317 Pub do not teach or suggest their combination of a data processor for simultaneous multithreaded processing, wherein the threads share a resource in which the resource keeps track of a how many times the first entry of a thread passes the last entry of the same thread in order to efficiently use memory and to keep track of the order of instructions in an out-of-order processor.

Attorney for Applicants thank the Examiner for his careful review of the specification, the figures, and the claims. Applicants have thus amended the specification and the claims to remove the objections and the rejections of the claims under 35 U.S.C. §112, second paragraph. In a separate paper, Applicants submit a Proposed Amendment to the Drawing. Having reviewed the art submitted by the Examiner, Attorney for Applicants is confident of the patentability of the claimed invention herein. Multithreaded processing having hardware resources shared by more than one thread and keeping track of the order of the resources allocated to each thread by allowing a head pointer to surpass a tail pointer and then keeping track of the number of passes in an out-of-order processor is not trivial, is not a mere combination of several references, and is not an obvious modification of one or more references. Applicants thus respectfully request the Examiner to reconsider the application in view the amendments and remarks, and pass the application to issuance. The Examiner is further invited to telephone the Attorney listed below if he thinks it would expedite the prosecution and the issuance of the patent.

Respectfully submitted,
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